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EXAMINER

JORGENSEN, LELAND R

ART UNIT PAPER NUMBER

2675

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

09/823,927

**Applicant(s)**

TSUTSUI ET AL.

**Examiner**

Leland R. Jorgensen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 18 March 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1 - 31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 - 31 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 103***

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
2. Claims 1 and 15 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over West et al., USPN 5,537,650, in view of Nobuoka, USPN 5,552,836.

### **Claims 1 and 15 - 23**

West teaches a driving apparatus for a display device [147]. West, figures 5 and 6. The driving apparatus has a driving circuit for generating a signal to allow a display section to display. The driving circuit has a digital signal processing circuit for processing a digital signal, a digital-to-analog converter circuit [DAC 102, 104, and 106] for converting a digital signal to an analog signal, and an analog signal processing circuit for processing an analog signal. West, col. 2, lines 26 – 31; col. 7, line 55 – col. 8, line 47; col. 9, line 46 – col. 10, line 15; and figures 5 and 6. West teaches a power supply circuit [logic sub-circuit 110] for generating a supply voltage for the driving circuit. West, col. 8, lines 14 – 18, and figure 5. When a predetermined power save is instructed, the power system generates zero voltage during a blanking period and a normal voltage during the non-blanking period, so that the display picture still would display yet the drive would use less power. West, col. 3, lines 49 – 64; col. 9, lines 26 – 44. In other words, West teaches a power system that provides a voltage that is at a normal level during the non-blanking periods and an essentially zero level voltage during the blanking periods. West, col. 2,

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lines 5 – 23; col. 3, lines 40 – 48; col. 4, lines 23 – 39; col. 4, line 6 – col. 5., line 1; col. 6, lines 19 – 23; col. 7, lines 29 – 41; and col. 8, lines 14 – 18.

West teaches that the voltage is alternated between a normal voltage and a essentially zero voltage. West does not specifically teach that the power supply circuit reduces the supply voltage to a non-zero voltage supplied to said digital-to-analog converter circuit and to said analog signal processing circuit, from the supply voltage during the normal operation.

Nobuoka teaches a image signal processing circuit having a power supply circuit that reduces the supply voltage to a non-zero voltage supplied to a digital-to-analog converter circuit [A/D Converter 12] and to an analog signal processing circuit, from the supply voltage during the normal operation. Nobuoka, col. 1, line 64 – col. 2, line 16; col. 3, lines 38 – 44; col. 4, lines 4 – 20; and figure 4.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the non-zero voltage as taught by Nobuoka with the driving apparatus as taught by West to keep the digital-to-analog converted circuit from becoming unstable. Nobuoka invites such combination by teaching,

If there is no problem in the operation of the A/D converter 12 and the line memories 14 and 16 by turning on and off the power supply, the power supply is completely turned off during the vertical blanking period. If the operation of the above-described devices becomes unstable when the power supply is turned back on, the power supply is turned on earlier by a time required for stabilizing the operation during the vertical blanking period. Alternatively, the A/D converter 12 and the line memories 14 and 16 are placed in a standby state in which power consumption is small enough so that the circuits are capable of achieving stable operation after the vertical blanking period.

Nobuoka, col. 4, lines 10 – 20.

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3. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over West in view of Nobuoka as applied to claim 1 above, and further in view of Iwamoto et al., USPN 4,544,912.

**Claim 8**

West does not specifically teach the details of the digital-to-analog converter circuit.

West does not teach that the digital-to-analog converter circuit that includes a plurality of voltage dividing resistive elements connected in series to the power supply from the power supply circuit.

Iwamoto teaches an digital-to-analog converter circuit that includes a plurality of voltage dividing resistive elements connected in series to the power supply from the power supply circuit, divides the supply voltage into a plurality of stages by the voltage dividing resistive elements, selects a divided voltage corresponding to the digital data, and outputs an analog signal. Iwamoto, col. 1, lines 11 – 16; col. 3, lines 3 – 26; and figure 3.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the digital-to-analog converter as taught by Iwamoto with the driving apparatus as taught by West. Iwamoto invites such combination by teaching,

The present invention relates to a digital-to-analog converter (D/A converter). The D/A converter according to the present invention is used in, for example, an analog-to-digital conversion device of a step-by-step comparison type for processing signals in electronic circuit devices.

Iwamoto, col. 1, lines 11 – 16. Iwamoto discusses the disadvantages of prior art D/A converters.

Of a first prior art D/A converter, Iwamoto teaches,

However, such a prior art device is disadvantageous because another D/A converter must be provided to produce a variable reference voltage signal  $V_{ref}$  which is supplied to the D/A converter of FIG. 1 in order to effect analog control of the full-scale value  $V_f$ , and hence this prior art D/A converter device is very complicated.

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Iwamoto, col. 2, lines 8 – 11. Of a second D/A converter, Iwamoto teaches,

However, this prior art device is disadvantageous since it is difficult to carry out the automatic switching between the feedback resistors  $R_0$  and  $R_0'$  using a digital signal, because it is necessary to change the connection of the connecting conductor W which connects the output of the AMP to one of the feedback resistors  $R_0$  and  $R_0'$ . This method of controlling the full-scale value of the D/A converter of FIG. 2 is time-consuming and inconvenient.

Iwamoto, col. 2, lines 50 – 58. Iwamoto concludes,

An object of the present invention is to eliminate the above described disadvantages in prior art D/A converters of the resistor network type.

Iwamoto, col. 3, lines 3 – 5.

4. Claims 2, 3, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over West and Nobuoka as applied to claim 1, or over West in view of Iwamoto and Nobuoka as applied to claim 8 above, and further in view of Volk, USPN 6,087,816, and Brooks et al., USPN 4,347,474.

#### **Claims 2 and 9**

Neither West nor Iwamoto teach the details of the power supply circuit.

Volk teaches the details of a power supply circuit. Specifically, Volk teaches a power supply circuit that comprises a boosting section [transistors PFET and NFET, inductor L, diodes D1 and D2, and capacitors C1 and C2] for boosting the input voltage [ $V_{in}$ ] and a feedback section [resistors R1 and R2, comparator, Clock pulse generator, and PWM Control State Machine] for detecting the supply voltage [ $V_{out}$ ] at the output end of the power supply as a resistor divided voltage, comparing the detected voltage with a reference voltage [ $V_{ref}$ ], and

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controlling the boosting section so that the supply voltage is constant. Volk, col. 3, lines 14 50; and figure 2. Compare figure 4 and page 15, lines 14 – 21 of the specifications.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the power supply circuit as taught by Volk with the driving apparatus as taught by West or by West in view of Iwamoto. Volk invites such combination by teaching,

Voltage regulators of various types are well known in the prior art. Of particular importance to the present invention are switching regulators which allow the regulators to provide a regulator output of a voltage which can be either higher or lower than the input voltage, as desired or as required for a particular application. One application for such regulators is with respect to systems operating on rechargeable batteries such as, by way of example, lap top computers. In this application, a charged battery may provide an input voltage to the regulator exceeding the desired regulated output voltage thereof, though with the battery voltage sagging to a voltage below the desired output voltage of the regulator as the battery discharges. The time between recharges necessary in such an application may be extended if the system will operate on a significantly reduced battery output voltage until such time as the battery is nearly fully discharged. The time between recharges can also be extended if the efficiency of the regulator in such a system is improved and, of course, the size of various components of the regulator, such as the inductor, can be decreased with such increased efficiency because of the proportionately lower power dissipation in the regulator. Similarly, battery powered systems such as laptop computers may be operable with different types of batteries or battery packs having different output voltages, some requiring step-up and some step-down in the battery voltage to provide the desired regulated voltage for system operation. Also such systems are often operable on a battery pack or an AC-to-DC converter, the two frequently having significantly different voltages to present to the regulator. These are merely exemplary of the many applications in which this type of regulator is useful, if not mandatory.

Volk, col. 1, lines 10 – 42. Volk adds the following advantages,

Step-up/step-down switching regulators and pulse width modulation control therefor which can provide a high output current, high efficiency, use a physically smaller inductor and physically smaller transistors, have lower output voltage ripple, excellent line and load regulation stability and very fast transient response. The modulation control includes three operating states. The improved operating characteristics are obtained by including, as one of the operating states, the direct flow of current from the input of the regulator to the output of the

regulator. This allows delivery of current from the inductor to the output a greater percentage of the time than in the prior art.

Volk, col. 2, lines 41 – 52.

Neither West, Iwamoto, nor Volk teach that the resisters have a switch.

Brooks teaches a plurality of resistive elements [resistors 28 and 32] connected to the output end of the power supply for detecting the supply voltage. A selector switch [inherent to potentiometer 30] for selecting a resistive element are connected to the feedback section from among the plurality of resistive elements. The divided voltage value of the supply voltage input to the feedback section is adjusted in response to the resistance value of the resistive element selected by the selector switch, and the output supply voltage is changed. Brooks, col. 3, lines 17 – 41, and figure 1.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the power supply circuit switch as taught by Brooks with the driving apparatus as taught by Volk and by West or West in view of Iwamoto. Brooks invites such combination by teaching,

It is an object of the present invention to provide a power transformer which overcomes the environmental problems associated with conventional power transformers.

Another object of the present invention is to provide solid state (semiconductor) apparatus which provides many of the functional characteristics of the conventional power transformer while having the advantages of solid state circuitry.

Another object of the present invention is to provide solid state apparatus which provides variable step up or step down voltage transformation.

A further object of the present invention is to provide a solid state transformer having automatic voltage regulation with varying loads and leading and lagging power factors.



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Still another object of the present invention is to provide a solid state transformer having high efficiency high reliability, and superior voltage regulation, independent of load diversity.

Brooks, col. 2, lines 20 - 39.

### **Claims 3 and 10**

Yolks teaches that a resistive element with a lower resistance value is selected by the selector switch when reduction in the output supply voltage is desired so that the divided voltage value input to the feedback section is increased. Yatabe, col. 3, lines 17 - 50.

5. Claims 4, 5, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over West and Nobuoka as applied to claim 1 above or over West in view of Nobuoka and Iwamoto as applied to claim 8 above, and further in view of Nakanishi, USPN 6,323,851 B1.

### **Claims 4 and 11**

Claims 4 and 11 each add details to the power supply circuit.

Neither West nor Iwamoto teach these details.

Nakanishi teaches a power supply circuit [power source circuit 21] that comprises a boosting section [booster circuit 210] for boosting the input voltage, a boosted power supply output switch [switch controller 213] for controlling passage between the boosting section and the output end of power supply, and a non-boosted power supply output switch [SW9] for bypassing the input and the output ends of power supply. Nakanishi, col. 4, line 34 – col. 5, line 48; col. 6, lines 12 – 59; col. 10, lines 49 – 57; and figure 2.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the power supply circuit as taught by Nakanishi with the driving apparatus as taught

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by West or West in view of Iwamoto so that the two types of output switches are switched and controlled such that one of the boosted or non-boosted supply voltages is output to the digital-to-analog converter circuit and to the analog signal processing circuit. Nakanishi invites such combination by teaching,

The present invention relates to a circuit and a method for driving a display device, more particularly to a circuit and a method for driving a display device which can prevent undesired bright lines or spots from appearing on a display screen when power supply is cut off.

Nakanishi, col. 1, lines 6 – 10. Nakanishi adds,

A display device is driven with a voltage which is higher than a source voltage supplied from a battery or the like. To obtain such a drive voltage, a drive circuit of the display device comprises a booster circuit for boosting a source voltage from a battery or the like up to a plurality of predetermined high voltages. The drive circuit has its power source circuit and it outputs a plurality of different voltages because the display device needs different voltages to its scanning electrodes and signal electrodes for time-sharing addressing.

A booster circuit or a dividing circuit is used as such a power source circuit which outputs a plurality of different voltages. The booster circuit boosts a source voltage into a plurality of different voltages. The booster circuit boosts a voltage by switching connection of a plurality of capacitors so that charged voltages in the capacitors are added to each other. The dividing circuit divides a previously boosted voltage into a plurality of different voltages. The dividing circuit divides a boosted source voltage with a series circuit of resistors or capacitors.

A capacitor-based booster or dividing circuit is advantageous to reduce its power consumption.

Nakanishi, col. 1, lines 13 – 34. Nakanishi teaches the following objects and advantageous.

The present invention has been made in consideration of the above, and it is an object to prevent irregular display caused by power-off action of the device from occurring.

It is another object of the present invention to terminate activity of the display device without irregular display after the device is turned off.

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Nakanishi, col. 1, lines 53 – 58. Nakanishi further adds,

In the above embodiments, the following steps are taken. Discharging the capacitors, terminating the boost operation to reduce the boosted voltages and to terminate the output of the boosted voltages, and selecting a non-boosted voltage as a voltage to be applied. Those steps are performed in order to prevent irregular display during the off-state period from occurring and terminate display operation without occurrence of the irregular display.

Nakanishi, col. 10, lines 49 – 57. Nakanishi concludes with a description of its application to various types of displays.

The driving circuit of the present invention may be used for not only the LCD device but for a PDP (plasma display panel), an EL (electroluminescent) display, an FED (field emission display), or the like. In other words, the driving circuit of the present invention may be used for a display device in which capacitors generate drive voltages and charges in the capacitors may cause irregular display during the off-state period.

As described in the above, the present invention prevents irregular display from appearing on a display screen during an off-state period, thus, the display operation is terminated without occurrence of the irregular display.

Nakanishi, col. 13, lines 44 – 41.

### **Claims 5 and 12**

Nakanishi teaches a power supply circuit [power source circuit 21] that comprises a boosting section [booster circuit 210] for boosting the input voltage, a boosted power supply output switch [switch controller 213] for controlling passage between the boosting section and the output end of power supply, and a non-boosted power supply output switch [SW9] for bypassing the input and the output ends of power supply. Nakanishi, col. 4, line 34 – col. 5, line 48; col. 6, lines 12 – 59; col. 10, lines 49 – 57; and figure 2. The boosting section [booster circuit 210] includes a plurality of capacitors [boosting capacitors C-1 to C-4] and a plurality of switches [SW1 to SW8] for the capacitors, for boosting an input voltage by switching and

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controlling the plurality of switches for capacitors. Nakanishi, col. 4, line 34 – 57; and figure 2. A clock signal produced by the driving circuit is used for switching and controlling the plurality of switches for capacitors. Nakanishi, col. 12, lines 49 – 62. It is inherent that the clock signal is produced by a clock.

For the reasons stated in the discussion about claims 4 and 13, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the power supply circuit as taught by Nakanishi with the driving apparatus as taught by West or West in view of Iwamoto.

6. Claims 6, 7, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over West in view of Nobuoka and Nakanishi as applied to claim 5 above or over West in view of Iwamoto and Nobuoka and further in view of Nakanishi as applied to claim 12 above, and further in view of Niijima, USPN 5,155,840.

#### **Claims 6 and 13**

West and Nakanishi teach that the driving circuit determines a current mode from a boosted power supply generating mode, a non-boosted power supply generating mode, or a power supply suspension mode, based on a predetermined power save control instruction, and based on the determination controls supply and suspension of supply of the power supply clock or supply and suspension of supply of the clock, and opening/closing of the output switches of the power supply circuit.

Neither West, Nakanishi, nor Iwamoto teach that the clock signal is from an oscillation circuit.

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Nijjima teaches clock to generate signals from a oscillation circuit [Sub System-Clock Oscillation Circuit 4 and Main System-Clock Oscillation Circuit 5]. Nijjima, col. 5, lines 22 – 40; and figure 1.

It would have been obvious to one of ordinary skill in the art at the time of the invention have to combine the clock having an oscillation circuit with the driving apparatus as taught by West and Nakanishi or West, Nakanishi, or Iwamoto. Nijjima invites such combination by teaching,

The present invention relates to a single-chip microcomputer which possesses internally a clock-signal switching function and, more particularly, to a single-chip microcomputer capable of automatically stopping the oscillation of a main system-clock oscillation circuit after a clock signal has been switched to a sub clock-signal from a main clock-signal.

Today, one of the capabilities which is sought in a single-chip microcomputer is that of reducing power consumption.

A conventional example in which an attempt has been made to reduce power consumption is one which employs two oscillators, one being a main system-clock oscillator for a high speed operation and the other being a sub system-clock oscillator for a low speed operation.

In this conventional example, during the period in which the single-chip microcomputer is operable by the clock-signal for a low speed operation, the main system-clock oscillation circuit stops its operation and only the sub system-clock oscillation circuit which is slow in speed but in which the power consumption is small operates. Such a conventional single-chip microcomputer and a problem therein are fully explained later for assisting the understanding of the present invention.

Nijjima, col. 1, lines 8 – 32. Nijjima teaches as an object of the invention,

It is, therefore, an object of the present invention to overcome the problem existing in the conventional arrangement and to provide an improved single-chip microcomputer.

It is another object of the present invention to provide a single-chip microcomputer which is capable of effecting an automatic stop of a main system-

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clock oscillation circuit after a main clock-signal has been switched to a sub clock-signal.

Niijima, col. 1, lines 35 - 44.

### **Claims 7 and 14**

Nakanishi teaches a power supply circuit [power source circuit 21] that comprises a boosting section [booster circuit 210] for boosting the input voltage, a boosted power supply output switch [switch controller 213] for controlling passage between the boosting section and the output end of power supply, and a non-boosted power supply output switch [SW9] for bypassing the input and the output ends of power supply. Nakanishi, col. 4, line 34 – col. 5, line 48; col. 6, lines 12 – 59; col. 10, lines 49 – 57; and figure 2. The boosting section [booster circuit 210] includes a plurality of capacitors [boosting capacitors C-1 to C-4] and a plurality of switches [SW1 to SW8] for the capacitors, for boosting an input voltage by switching and controlling the plurality of switches for capacitors. Nakanishi, col. 4, line 34 – 57; and figure 2. A clock signal produced by the driving circuit is used for switching and controlling the plurality of switches for capacitors. Nakanishi, col. 12, lines 49 – 62. It is inherent that the clock signal is produced by a clock.

For the reasons stated in the discussion about claims 4 and 13, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the power supply circuit as taught by Nakanishi with the driving apparatus as taught by West or West in view of Iwamoto.

Niijima teaches clock to generate signals from a oscillation circuit [Sub System-Clock Oscillation Circuit 4 and Main System-Clock Oscillation Circuit 5]. Niijima, col. 5, lines 22 – 40; and figure 1.

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For the reasons stated above in the discussion about claims 6 and 13, it would have been obvious to one of ordinary skill in the art at the time of the invention have to combine the clock having an oscillation circuit with the driving apparatus as taught by West and Nakanishi or West, Nakanishi, or Iwamoto.

7. Claims 24 - 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over West in view of Nobuoka as applied to claims 1, 15, 16, or 18 above, and further in view of Brill et al., USPN 6,078,319.

Both West and Nobuoka teach a reduced voltage only during the blanking period. Thus, neither West nor Nobuoka teach that the voltage is reduced during a period when the display data is written to the display region, or when the digital-to-analog converter outputs and analog signal corresponding to a digital signal.

Bril teaches a power save mode that delivers a reduced voltage to a driving circuit [core circuitry 170 and output circuitry 180 for display 130]. Bril, col. 2, lines 4 – 11, 56 – 61; col. 4, lines 29 – 39; and figure 1.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the reduced power save mode as taught by Bril with the driving apparatus as taught by West and Nobuoka to produce a video display that has a reduced power consumption. Specifically it would have been obvious to use the digital-to-analog converter circuit as taught in West and Nobuoka as the core circuitry taught by Bril. Bril teaches that “Core circuitry 170 may retrieve video data from video memory 120 and convert the video data into output data.” Bril,

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col. 2, lines 62 – 63. This is what the digital-to-analog converter circuit and the analog signal processing circuit do. Bril invites such combination by teaching,

It is an object therefor to switch from a first supply voltage to a second supply voltage in response to performance demands of an integrated circuit.

It is a further object of the present invention to output a voltage selection signal in response to performance demands of an integrated circuit.

It is a further object of the present invention to output a voltage selection signal in response to different pixel resolutions or video modes in a video controller circuit.

It is a further object of the present invention to reduce power consumption in an integrated circuit.

Bril, col. 2, lines 12 – 23. Bril adds,

It should be noted that the present invention is intended for use in a integrated circuit constructed using a technology which may operate at multiple supply voltages (e.g., CMOS technology). Moreover, such a technology may be limited to operating at slower clock speed at lower voltages. Since lower clock speed may limit performance, the present invention allows an integrated circuit to operate at these lower supply voltages (and lower clock speeds) when permissible, switching to higher voltages when performance requirements dictate the need for higher clock speeds.

Bril, col. 6, lines 4 – 13.

### ***Response to Arguments***

8. Applicant's arguments with respect to claims 1 - 18 have been considered but are moot in view of the new ground(s) of rejection.



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***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Obitsu, UPSN 6,380,982, teaches a power save operation for an A/D converter.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland R. Jorgensen whose telephone number is 571-272-7768. The examiner can normally be reached on Monday through Friday, 10:00 am through 6:00 pm.. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

lrj

  
**KENT CHANG**  
**PRIMARY EXAMINER**